

SPECIFICATION

TO WHOM IT MAY CONCERN:

Be it known that we, with names, residence, and citizenship listed below, have invented the inventions described in the following specification entitled:

**METHODS AND APPARATUS FOR MONITORING FREQUENCY
CORRECTIONS IN A CLOCK AND DATA RECOVERY PHASE-LOCK LOOP,
AND FOR DERIVING OPERATING INDICATIONS THEREFROM**

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**METHODS AND APPARATUS FOR MONITORING FREQUENCY
CORRECTIONS IN A CLOCK AND DATA RECOVERY PHASE-LOCK
LOOP, AND FOR DERIVING OPERATING INDICATIONS THEREFROM**

Background

[0001] During the operation of a clock and data recovery phase-lock loop, anomolous events in a received data stream may require the loop to make transient frequency corrections in the recovered clock. Exemplary anomolous events are phase and/or frequency steps in the received data stream.

[0002] During the time the phase-lock loop is responding to an anomolous event, the error rate in recovered data can be expected to rise. Some means to infer the existence and/or magnitude of such error would be desirable.

Summary

[0003] One aspect of the invention is embodied in a method wherein the number of up and down frequency corrections made by a phase-lock loop are monitored. For each of a number of time periods, the numbers of up and down frequency corrections made by the phase-lock loop during the time period are netted together. One or more operating indications are then derived from the net numbers.

[0004] Another aspect of the invention is embodied in apparatus comprising an accumulator stage, a timer and some logic. The accumulator stage i) receives up and down frequency corrections from a clock and data recovery phase-lock loop, and then ii) for each of a number of time periods, nets together the numbers of up and down frequency corrections that were received during the time period. The timer resets the accumulator at the start of each time period. The logic compares each net number to one or more thresholds and provides one or more operating indications based on the comparisons.

[0005] Other embodiments of the invention are also disclosed.

Brief Description of the Drawings

[0006] Illustrative and presently preferred embodiments of the invention are illustrated in the drawings, in which:

[0007] FIG. 1 illustrates an exemplary method for monitoring frequency corrections in a clock and data recovery phase-lock loop, and for deriving operating indications therefrom; and

[0008] FIG. 2 illustrates exemplary apparatus for monitoring frequency corrections in a clock and data recovery phase-lock loop, and for deriving operating indications therefrom.

Description of the Invention

[0009] The error rate in data that is recovered by a clock and data recovery phase-lock loop should be roughly equivalent to the integrated frequency correction made by the phase-lock loop over a given time period. The method and apparatus illustrated in FIGS. 1 & 2 therefore provide means for monitoring frequency corrections in a clock and data recovery phase-lock loop, and for deriving operating indications (e.g., status and/or error indications) therefrom. In this manner, the existence and/or magnitude of the error rate in recovered data can be inferred.

[0010] The frequency corrections provided by a phase-lock loop are typically provided in the form of “up” and “down” voltage corrections (although other forms of correction are possible). As a result, the method 100 (FIG. 1) begins with the monitoring 102 of up and down frequency corrections made by a phase-lock loop. For each of a number of time periods, the numbers of up and down frequency corrections made by the phase-lock loop during the time period are netted together 104. These net numbers are then used 106 to derive one or more operating indications.

[0011] Optionally, the method 100 may de-serialize the monitored frequency corrections to form parallel “words” of frequency corrections. In this manner, the netting of frequency corrections may be undertaken at a frequency that is less than the operating frequency of the phase-lock loop. For example, if ten consecutive frequency corrections are merged into a 10-

bit word, then the netting of frequency corrections can be undertaken at a frequency that is an order of magnitude less than the operating frequency of the phase-lock loop. Note that the time period over which frequency corrections are netted may be long enough to require the netting of frequency corrections contained in multiple parallel words.

[0012] Various operating indications may be derived, in various ways. By way of example, these operating indications may take the form of error and/or status indications. In one embodiment of the method 100, an error indication is generated whenever one of the net numbers is non-zero. In another embodiment, each net number is compared to one or more thresholds and, if any of the net numbers exceeds one of the thresholds, an error indication is generated. By way of example, the one or more thresholds could comprise a single threshold to which an absolute value of netted frequency corrections is compared. Or, the one or more thresholds could comprise positive and negative thresholds of different values to which a signed (i.e., positive or negative) net number is compared.

[0013] One way to generate an indication of whether a net number exceeds a threshold is to set a built-in self-test (BIST) sticky bit. BIST hardware may then be used to read the sticky bit and provide an error or status indication to a user, software or firmware that can determine how to handle same. In some embodiments, it may be desirable to have software or firmware make automatic adjustments to a phase-lock loop, in response to a received operating indication.

[0014] In yet another embodiment of the method 100, each net number is compared with a maximum of previously encountered net numbers. If a net number exceeds the maximum net number, the maximum net number is set to the net number that exceeds it. The maximum net number is then provided as an error or status indication.

[0015] The method 100 may further comprise outputting each of the net numbers. By way of example, the net numbers may be output to BIST hardware and then read therefrom.

[0016] The operating indications noted above may be used, for example, to infer the following. If a net number of frequency corrections in a given time period is non-zero, there is a greater chance that anomolous events in a received data stream are leading to errors in the data that is being recovered from the received stream. However, it may be decided that a given projected error rate is tolerable. In such a case, it may be desirable to set a non-zero threshold (or even set positive and negative thresholds) so that small net frequency corrections will not trigger an error indication. It is also possible that the tolerable error rate is not known. If not known, it may be useful to update and store a maximum net number, or even output each of the net numbers that are calculated. Very large net frequency corrections are likely to be indicative of a problem in the function of the phase-lock loop itself.

[0017] Exemplary apparatus 200 for monitoring frequency corrections in a clock and data recovery phase-lock loop 202, and for deriving operating indications therefrom, is shown in FIG. 2. In general, the apparatus 200

comprises an accumulator stage 206, a timer 212, and some logic 210. The accumulator stage 206 i) receives up and down frequency corrections from the phase-lock loop 202, and then ii) for each of a number of time periods, nets together the numbers of up and down frequency corrections that were received during the time period. The timer 212 resets the accumulator stage 206 at the start of each time period. The logic 210 compares the net numbers to one or more thresholds and then provides one or more operating indications based on the comparisons.

[0018] Optionally, a de-serializing stage 204 may be provided between the phase-lock loop 202 and the accumulator stage 206. In this manner, sets of the up and down frequency corrections may be provided to the accumulator stage 206 as parallel words of frequency corrections.

[0019] The apparatus 200 may also comprise a capture stage 208 to capture net numbers from the accumulator stage 206 and, at the end of each time period, provide a net number to the logic 210. The capture stage 208 is useful in preserving a net number after the accumulator stage 206 has begun compiling the net number for a next time period. In one embodiment of the apparatus 200, net numbers stored by the capture stage 208 are dumped to BIST hardware 218.

[0020] The accumulator stage 206, capture stage 208, timer 212 and logic 210 may all be clocked by a test clock (TEST CLK) having a frequency that is lower than that of the phase-lock loop 202. This is made possible, in part, by the de-serializing of frequency corrections into parallel words of

frequency corrections.

[0021] The timer 212 may serve to not only reset the accumulator stage 206 but, after a delay, also reset the capture stage 208. In one embodiment, the timer 212 is implemented as a rollover counter.

[0022] The logic 210 may perform one or more of a number of functions.

In one embodiment, the logic 210 determines whether any net number it receives is non-zero. If so, it provides an error indication by, for example, setting a BIST sticky bit 216. In another embodiment, the logic 210 provides an error indication if a net number exceeds any one of a plurality of thresholds, such as positive and negative thresholds. Again, this error indication may be provided by setting a BIST sticky bit 216.

[0023] In yet another embodiment, the logic 210 sets a threshold equal to a net number if the net number exceeds the threshold. In this manner, a threshold provides an indication of the maximum net frequency correction made by the phase-lock loop 202.

[0024] The output of logic 210 may also drive other registers, storage cells and/or logic, some of which may or may not be driven via the test clock (TEST CLK).

[0025] While illustrative and presently preferred embodiments of the invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed, and that the appended claims are intended to be construed to include such variations, except as limited by the prior art.